



A5N:300.XXH

VOLTAGE RATINGS

Part Number	V _{RRM} , V _R (V) Max. rep. peak reverse voltage		V _{RSM} , V _R (V) Max. non- rep. peak reverse voltage
	T _J = 0 to 125°C	T _J = -40 to 0°C	T _J = 25 to 125°C
A5N:300.12H	1200	1200	1300
A5N:300.14H	1400	1400	1500
A5N:300.16H	1600	1600	1700
A5N:300.18H	1800	1800	1900
A5N:300.20H	2000	2000	2100

MAXIMUM ALLOWABLE RATINGS

PARAMETER	VALUE	UNITS	NOTES
T _J Junction Temperature	-40 to 125	°C	-
T _{stg} Storage Temperature	-40 to 150	°C	-
I _{T(AV)} Max. Av. current @ Max. T _C	300	A	180° half sine wave
	75	°C	
I _{T(RMS)} Nom. RMS current	470	A	-
I _{TSM} Max. Peak non-rep. surge current	4.53	kA	50 Hz half cycle sine wave Initial T _J = 125°C, rated V _{RRM} applied after surge.
	4.94		60 Hz half cycle sine wave
	5.23		50 Hz half cycle sine wave Initial T _J = 125°C, no voltage applied after surge.
	5.70		60 Hz half cycle sine wave
I ² t Max. I ² t capability	109	kA ² s	t = 10ms Initial T _J = 125°C, rated V _{RRM} applied after surge.
	119		t = 8.3 ms
	125		t = 10ms Initial T _J = 125°C, no voltage applied after surge.
	136		t = 8.3 ms
I ^{2,1/2} Max. I ^{2,1/2} capability	1490	kA ² s ^{1/2}	Initial T _J = 125°C, no voltage applied after surge. I ² t for time t _x = I ^{2,1/2} * t _x ^{1/2} . (0.1 < t _x < 10ms).
di/dt Max. Non-repetitive rate-of- rise current	800	A/ s	T _J = 125°C, V _D = V _{DRM} , I _{TM} = 1600A. Gate pulse: 20V, 20 , 10 s, 0.5 s rise time, Max. repetitive di/dt is approximately 40% of non-repetitive value.
P _{GM} Max. Peak gate power	10	W	tp < 5 ms
P _{G(AV)} Max. Av. gate power	3	W	-
+I _{GM} Max. Peak gate current	150	mA	tp < 5 ms
-V _{GM} Max. Peak negative gate voltage	2	V	-
F Mounting Force	450	N.m	-



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CHARACTERISTICS

PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{TM} peak on-state voltage	---	---	1.93	V	Initial $T_J = 25^\circ\text{C}$, 50-60Hz half sine, $I_{peak} = 924\text{A}$.
$V_{T(TO)}$ Threshold voltage	---	---	0.88	V	$T_J = 125^\circ\text{C}$ Av. power = $V_{T(TO)} * I_{T(AV)} + r_T * [I_{T(RMS)}]^2$, 180° Half Sine.
r_T Slope resistance	---	---	1.28	m	Use low values for $I_{TM} < \text{rated } I_{T(AV)}$
I_L Latching current	---	---	400	mA	$T_C = 125^\circ\text{C}$, 12V anode. Gate pulse: 10V, 20 , 100 s.
I_H Holding current	---	---	500	mA	$T_C = 25^\circ\text{C}$, 12V anode. Initial $I_T = 15\text{A}$.
t_d Delay time	---	0.7	1	s	$T_C = 25^\circ\text{C}$, $V_D = V_{DRM}$, 50A resistive load. Gate pulse: 10V, 20 , 10 s, 1 s rise time.
t_q Turn-off time	---	---	100	s	$T_J = 125^\circ\text{C}$, $I_{TM} = 550\text{A}$, $di/dt = 40\text{A/s}$, $V_R = 50\text{V}$. $dv/dt = 20\text{V/s}$ lin. to rated V_{DRM} . Gate: 0V, 100 .
dv/dt Critical rate-of-rise of off-state voltage	---	---	1000	V/ s	$T_J = 125^\circ\text{C}$, Exp. To 67% V_{DRM} , gate open.
I_{RM} , I_{DM} Peak reverse and off-state current	---	15	30	mA	$T_J = 125^\circ\text{C}$, Rated V_{RRM} and V_{DRM} , gate open.
I_{GT} DC gate current to trigger	---	---	360	mA	$T_C = -40^\circ\text{C}$
	---	---	180		$T_C = 25^\circ\text{C}$
V_{GT} DC gate voltage to trigger	6	---	---	V	$T_C = -40^\circ\text{C}$
	3	---	---		$T_C = 25^\circ\text{C}$
V_{GD} DC gate voltage not to trigger	---	---	0.3	V	$T_C = 25^\circ\text{C}$, Max. Value which will not trigger with rated V_{DRM} anode.
R_{thJC} Thermal resistance, junction-to-case	---	---	0.085	$^\circ\text{C/W}$	DC operation, double side cooled.
	---	---	0.106	$^\circ\text{C/W}$	180° sine wave, double side cooled.
	---	---	0.109	$^\circ\text{C/W}$	120° rectangular wave, double side cooled.
R_{thCS} Thermal resistance, case-to-sink	---	---	0.03	$^\circ\text{C/W}$	Mtg. Surface smooth, flat and greased. Double side cooled.
wt Weight	---	57(2.1)	---	g(oz.)	---
Case Style	TO-200AA			JEDEC	---

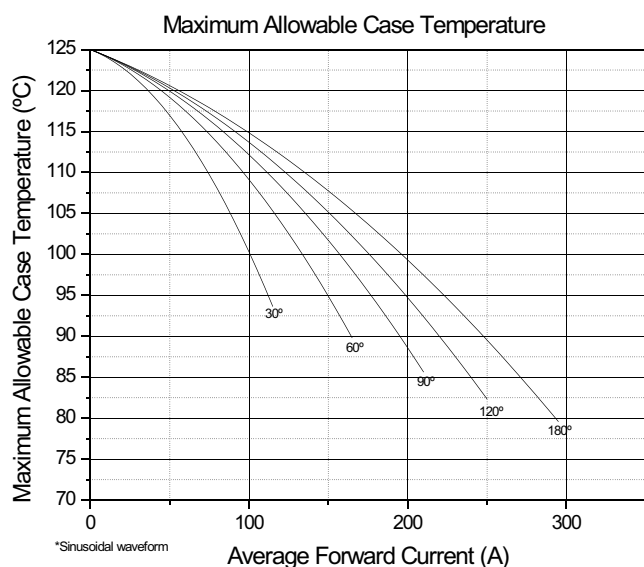


Fig. 1 - Current Ratings Characteristics

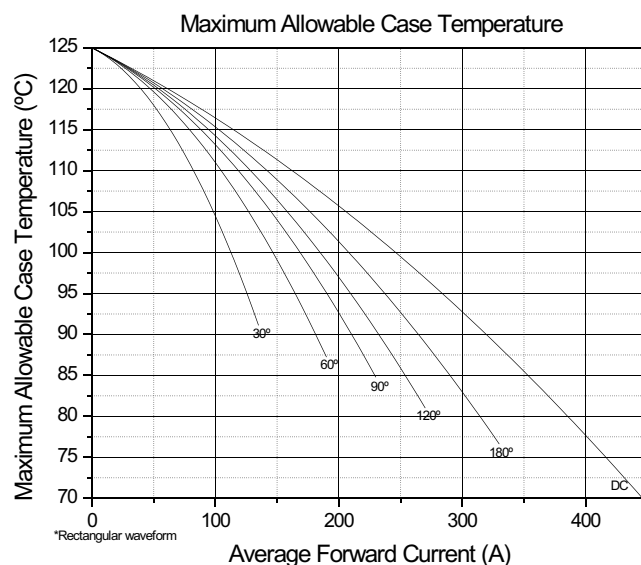


Fig. 2 - Current Ratings Characteristics



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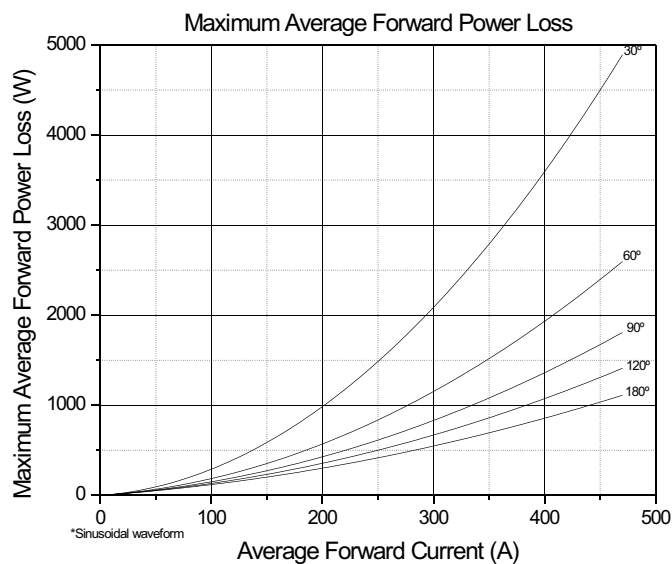


Fig. 3 - Forward Power Loss Characteristics

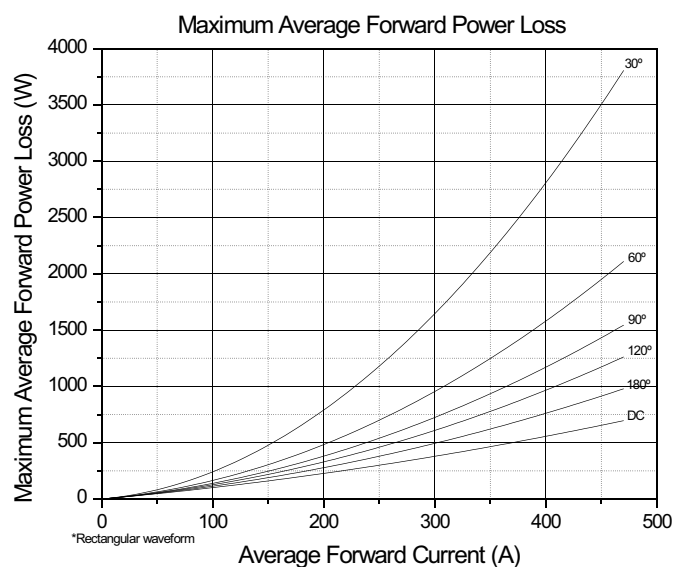


Fig. 4 - Forward Power Loss Characteristics

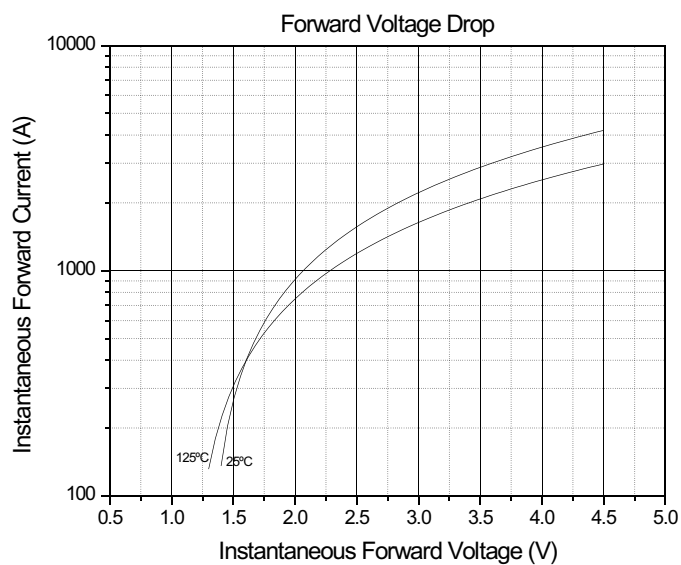


Fig. 5 - Forward Voltage Drop Characteristics

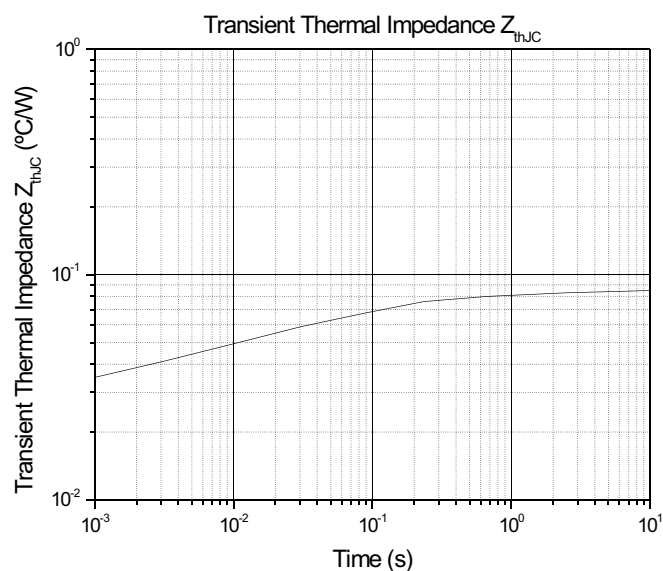


Fig. 6 - Transient Thermal Impedance Characteristics



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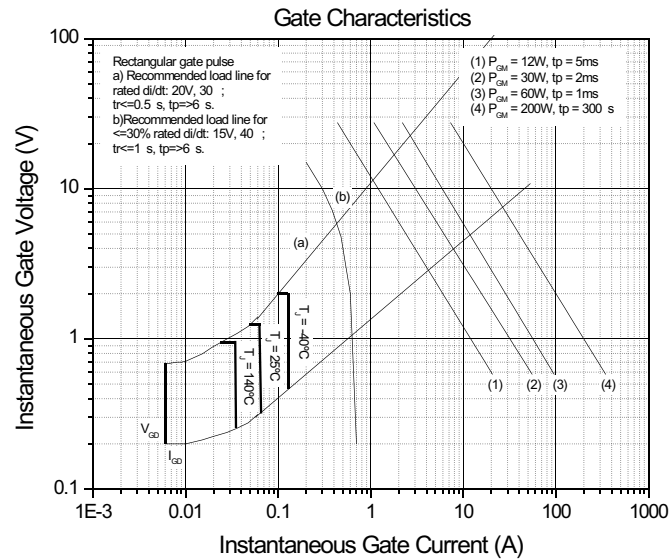


Fig. 7 - Gate Trigger Characteristics

TO-200AA

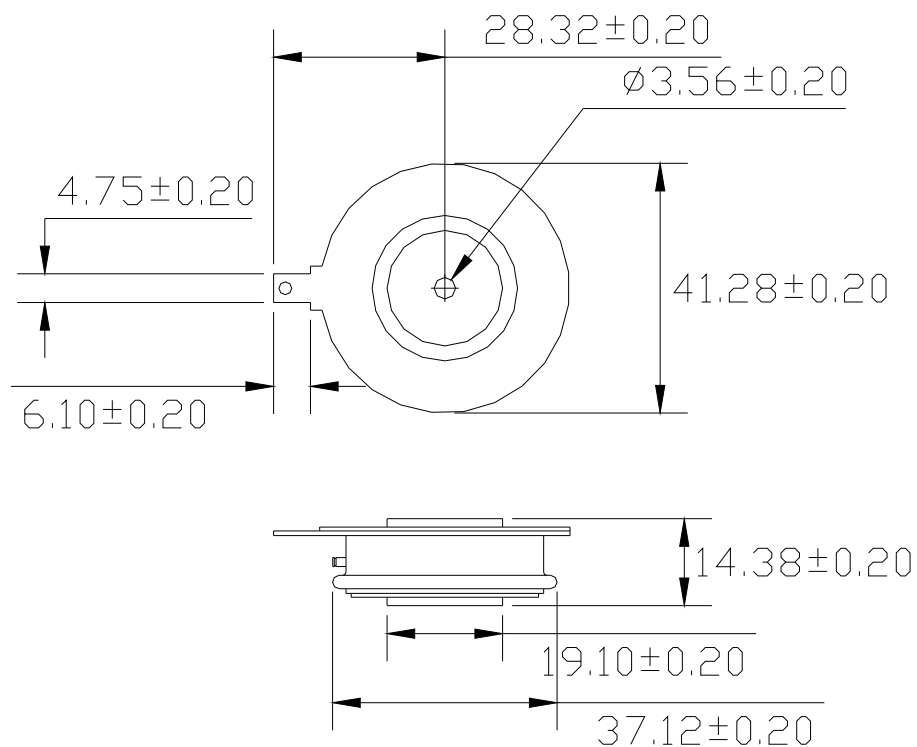


Fig. 8 - Outline Characteristics